

Claims

What is claimed is:

1. A semiconductor device comprising:

first and second contact pads;

a first plug portion electrically coupled with the first contact pad;

a capacitor bottom plate electrically coupled with the second contact pad;

a dielectric etch stop liner interposed between the bottom plate and the first plug portion;

a capacitor top plate having a portion which at least partially extends over the etch stop liner, wherein the top plate portion is further from the first contact pad than a top surface of the first plug portion, and wherein the top plate has an opening therein; and

a second plug portion electrically coupled with the first plug portion and extending through the opening in the top plate.

2. The semiconductor device of claim 1 further comprising a dielectric spacer which electrically separates the second plug portion from the capacitor top plate portion.

3. The semiconductor device of claim 1 wherein the bottom plate comprises, in cross section, at least two vertically-oriented portions which define a container, wherein at least part of each vertically-oriented portion of the bottom plate is interposed between two vertically-oriented portions of the top plate and is separated by the two vertically-oriented portions of the top plate by a capacitor cell dielectric layer to form a double-sided container capacitor.

4. The semiconductor device of claim 1 further comprising a capacitor cell dielectric layer which contacts the etch stop liner and the capacitor top plate.

5. The semiconductor device of claim 1 further comprising a receptacle defined by said capacitor top plate which is interposed between the first plug portion and the capacitor bottom plate.

6. The semiconductor device of claim 5 wherein the plug portion has a height, and a receptacle height is about 2/3 of the plug portion height.

7. An in-process semiconductor device, comprising:

a semiconductor wafer;

first and second contact pads, with each pad electrically coupled to the wafer;

a digit line plug portion electrically coupled with the first contact pad;

a first dielectric layer which contacts the digit line plug portion;

a photoresist layer which contacts the digit line plug portion, wherein the photoresist layer and the first dielectric layer electrically isolate the digit line plug portion from any other conductive layer except the first contact pad;

a second dielectric layer having an opening therein which exposes the second contact pad, wherein the second contact pad is free from contact with any conductive layer except the wafer.

8. The in-process semiconductor device of claim 7 wherein the second contact pad is a capacitor bottom plate contact pad.

9. The in-process semiconductor device of claim 8 wherein the in-process device comprises no conductive capacitor storage plate portion except the second contact pad.

10. The in-process semiconductor device of claim 7 further comprising an etch stop liner which contacts the first and second dielectric layers and the photoresist layer.

11. An in-process semiconductor device, comprising:

first, second, and third conductive contact pads;

a first container capacitor bottom plate electrically coupled with the first conductive contact pad, and a second container capacitor bottom plate electrically coupled with the second conductive contact pad, wherein the first and second container capacitor bottom plates each comprise at least one cross sectional free-standing vertically-oriented portion having an upper surface; and

a digit line contact plug interposed between the first and second container capacitor bottom plates and electrically coupled with the third conductive contact pad, wherein the digit line contact plug is free from contact with any conductive layer except the third conductive contact pad;

wherein the in-process semiconductor device comprises no container capacitor top plate layer.

12. The in-process semiconductor device of claim 11 further comprising an exposed etch stop liner having a first cross sectional portion interposed between the digit line contact plug and the first container capacitor bottom plate, and a second cross sectional portion interposed between the digit line contact plug and the second container capacitor bottom plate.

13. The in-process semiconductor device of claim 12 further comprising a dielectric layer having first cross sectional portion interposed between the digit line contact plug and the first cross sectional portion of the etch stop liner and a second cross sectional portion interposed between the digit line contact plug and the second cross sectional portion of the etch stop liner.

14. The in-process semiconductor device of claim 11 wherein the digit line contact plug comprises an upper surface which is at about an equal height with the upper surfaces of the cross sectional free-standing vertically-oriented portions of the first and second container capacitor bottom plates.